AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A network device~~, in particular~~ for a telecommunications network with synchronous digital hierarchy, for delay compensation of data packets, the network device comprising:

an input stage and an output state, where ~~which~~ delay occurs during passage of the data packets through ~~an~~ the input stage and ~~an~~ the output stage of the network device,

~~the output stage being connected to the input stage via~~ a first transfer path and ~~via~~ a second transfer path connecting the input stage to the output stage, where a first delay ~~occurring~~ occurs on the first transfer path and a second delay ~~occurring~~ occurs on the second transfer path, and where~~in~~ the data packets are transferred in multiplex frames, each containing at least one data packet to be transferred~~, as well as~~ and at least one phase reference identifier for determining the respective position of the data packet within the corresponding frame;~~,~~ ~~wherein the network device comprising~~

phase correcting means for adjusting the phase reference identifier allocated to a respective data packet by a predetermined phase correcting value, leading in the phase, which corresponds to a maximum expected delay for a transfer of the data packets on the first transfer path or the second transfer path;~~,~~ and

buffer means for buffering the data packets by buffering times such that for each respective data packet, ~~its~~ buffering time and ~~its~~ delay ~~actually~~ needed for passing through the network device, in total correspond to the maximum expected delay taken into account in ~~its~~ allocated, adjusted phase reference identifier of respective data packet.

2. (currently amended): A network device according to Claim 1, wherein the buffer means ~~determine~~ determines the delay of the data packets ~~actually~~ needed for passing through via the first transfer path or the second transfer path and adjust the respective buffering time to the ~~actually~~ needed delay.

3. (currently amended) A network device according to Claim 1, wherein the maximum expected delay is substantially determined ~~by means of~~ based on maximum lengths of connecting leads used for at least one of the first transfer path and~~/or~~ the second transfer path.

4. (original): A network device according to Claim 1, being constructed as a redundant network device wherein the first transfer path is guided via a first device and the second transfer path via a second device, redundant to the first device.

5. (original): A network device according to Claim 4, wherein the first device and the second device comprising a first or a second switching matrix, respectively.

6. (currently amended): A network device according to Claim 5, wherein the first switching matrix and the second switching matrix, each matrix comprising a first matrix module and a second matrix module, connected to one another via a connecting lead.

7. (original): A network device according to Claim 1, wherein the input stage and the corresponding output stage are combined into a joint module and/or the input stage and the output stage are constructed as matrix stages of a multi-stage switching matrix.

8. (original): A network device according to Claim 1, wherein the phase correcting means are allocated entirely or partially to the input stage or to the output stage.

9. (currently amended) A network device according to Claim 1, wherein the buffer means ~~comprise~~ comprises buffers arranged on one of: ~~the~~ an input side of the output stage, ~~or~~ on ~~the~~ an input side of the first transfer path, and ~~or~~ on the second transfer path.

10. (original): A network device according to Claim 1, wherein the multiplex frames are SDH frames and the phase reference identifiers are contained in the control information of the multiplex frames and the data packets are virtual containers or are transferred in virtual containers.

11. (currently amended): A method for delay compensation of data packets, ~~in particular~~ for a telecommunications network with synchronous digital hierarchy, which delay occurs during passage of the packets through a network device comprising an input stage and an output stage, connected to the input stage via a first transfer path and a second transfer path~~,~~; the method comprising:

transferring the data packets in multiplex frames, where a first delay ~~occurring~~ occurs on the first transfer path and a second delay ~~occurring~~ occurs on the second transfer path, and where ~~wherein the data packets are transferred in multiplex frames,~~ each of the multiplex frames contains ~~containing~~ at least one data packet to be transferred~~, as well as~~ and at least one phase reference identifier for determining the respective position of the data packet within the corresponding frame~~;~~; ~~wherein the network device performing the following steps:~~

adjusting the phase reference identifier allocated to a respective data packet by a predetermined phase correcting value, leading in the phase, which corresponds to a maximum expected delay for a transfer of the data packets on the first transfer path or the second transfer path~~;~~; and

buffering the data packets by buffering times such that for each respective data packet ~~its~~ buffering time and ~~its~~ delay ~~actually~~ needed for passing through the network device in total correspond to the maximum expected delay taken into account in ~~its~~ allocated, adjusted phase reference identifier.

12. (original): A program module for a network device comprising program code means which carry out the method according to Claim 11 when run by a control means of the network device.

13. (original): A memory means, in particular diskette, CD-ROM, Digital Versatile Disk, hard disk drive or similar, with a program module according to Claim 12 stored thereon.

14. (currently amended) A network device for processing digital data streams composed of frames, each containing at least one data packet and at least one corresponding phase reference identifier indicating the position of the data packet within its frame, the network device comprising:

compensation ~~means~~ module ~~for~~ compensating a delay of said data packet occurring during passage of the data packet through the network device, said compensation ~~means~~ module comprising:

phase correcting means for adjusting the phase reference identifier by a predetermined phase correcting value, which corresponds to a maximum expected delay for passage of the data packet through the network device and

buffer means for buffering the data packet for a predetermined buffering time such that ~~its~~ buffering time and ~~its~~ delay ~~actually~~ needed for passing through the network device in total correspond to the maximum expected delay.

15. (new): A network device for a telecommunications network with synchronous digital hierarchy, for delay compensation of data packets, the network device comprising:

an input stage having a first matrix unit and receiving data packets transferred in multiplex frames together with at least one phase reference identifier for determining the respective position of the data packet within the corresponding frame;

an output stage having a second matrix unit and receiving data packets of the multiplexed frames propagated within the network device; and

a first transfer path and a second transfer path connecting the input state to the output stage, where a first propagation delay occurs on the first transfer path and a second propagation delay occurs on the second transfer path,

wherein each of the first and second matrix units comprise:

a pointer processor adjusting the phase reference identifier allocated to a respective data packet by a predetermined phase correcting value, leading in the phase, which corresponds to a maximum expected delay for a transfer of the data packets on a longest transfer path out of the first transfer path and the second transfer path, and

a buffer buffering the data packets, where each data packet is buffered for a buffering time that corresponds to the maximum expected delay minus time needed to pass respective data packet through a respective transfer path,

wherein said buffering time is determined based on the adjusted phase reference identifier of the respective data packet.

16. (new): The network device according to claim 15, further comprising at least one intermediate stage, wherein the first transfer path and the second transfer path comprise multiple transfer paths connecting the input stage to a first intermediate stage, connecting the intermediate stages to each other, and connecting a last intermediate stage to the output stage, wherein each intermediate stage has a third matrix and wherein the third matrix comprises the pointer processor and the buffer.

17. (new): The network device according to claim 16, wherein the maximum expected delay is a value indicating longest time needed to propagate a data packet through a longest transfer path out of all multiple transfer paths within the network device.

18. (new): The network device according to claim 15, wherein the maximum expected delay is a value indicating longest time needed to propagate a data packet through the longest transfer path.